JC19 Rec'd PCT/PTO 18 JUL 2001

FORM PTO-1390 (Modified) (REV 11-2000) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER
83281

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR
09/889539

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/DE00/00270	**February 1, 2000**	**February 18, ~~2001~~** 1999

TITLE OF INVENTION
METHOD AND DEVICE FOR CALCULATING A DISCRETE ORTHOGONAL TRANSFORMATION SUCH AS FFT OR IFFT

APPLICANT(S) FOR DO/EO/US
Infineon Technologies AG
BACHER Martin

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☐ This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include itens (5), (6), (9) and (24) indicated below.
4. ☐ The US has been elected by the expiration of 19 months from the priority date (Article 31).
5. ☒ A copy of the International Application as filed (35 U.S.C. 371 (c) (2))
   a. ☐ is attached hereto (required only if not communicated by the International Bureau).
   b. ☒ has been communicated by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☒ An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. ☒ is attached hereto.
   b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4).
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3))
   a. ☐ are attached hereto (required only if not communicated by the International Bureau).
   b. ☐ have been communicated by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.
8. ☐ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☐ An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)).
10. ☐ An English language translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).
11. ☐ A copy of the International Preliminary Examination Report (PCT/IPEA/409).
12. ☐ A copy of the International Search Report (PCT/ISA/210).

Items 13 to 20 below concern document(s) or information included:

13. ☐ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
14. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
15. ☒ A **FIRST** preliminary amendment.
16. ☐ A **SECOND** or **SUBSEQUENT** preliminary amendment.
17. ☐ A substitute specification.
18. ☐ A change of power of attorney and/or address letter.
19. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 - 1.825.
20. ☐ A second copy of the published international application under 35 U.S.C. 154(d)(4).
21. ☐ A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
22. ☒ Certificate of Mailing by Express Mail
23. ☐ Other items or information:

PCTUS1/REV03

JC18 Rec'd PCT/PTO 1 8 JUL 2001

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
09/889539	PCT/DE00/00270	83281

24. The following fees are submitted:.

CALCULATIONS PTO USE ONLY

BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :

☒ Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO **$1000.00**

☐ International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO **$860.00**

☐ International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO **$710.00**

☐ International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4) **$690.00**

☐ International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) **$100.00**

				Calculations	PTO use only
ENTER APPROPRIATE BASIC FEE AMOUNT =				**$1,000.00**	
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☒ 30 months from the earliest claimed priority date (37 CFR 1.492 (e)).				**$130.00**	
CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	16 - 20 =	0	x $18.00	**$0.00**	
Independent claims	3 - 3 =	0	x $80.00	**$0.00**	
Multiple Dependent Claims **(check if applicable).**			☐	**$0.00**	
TOTAL OF ABOVE CALCULATIONS =				**$1,130.00**	
☐ Applicant claims small entity status. (See 37 CFR 1.27). The fees indicated above are reduced by 1/2.				**$0.00**	
SUBTOTAL =				**$1,130.00**	
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (f)). +				**$0.00**	
TOTAL NATIONAL FEE =				**$1,130.00**	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31) **(check if applicable).** ☐				**$0.00**	
TOTAL FEES ENCLOSED =				**$1,130.00**	
				Amount to be: refunded	$
				charged	$

a. ☒ A check in the amount of **$990.00** to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No. ______ in the amount of ______ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. **23-0920** A duplicate copy of this sheet is enclosed.

d. ☐ Fees are to be charged to a credit card. **WARNING:** Information on this form may become public. **Credit card information should not be included on this form.** Provide credit card information and authorization on PTO-2038.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

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NAME

27,466
REGISTRATION NUMBER

DATE

83281 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re U.S. Patent Application

Applicant: Infineon Technologies

Serial No.: Not Yet Assigned

Filed: Herewith

For: **METHOD AND DEVICE FOR CALCULATING A DISCRETE ORTHOGONAL TRANFORMATION SUCH AS FFT OR IFFT**

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

This is a Preliminary Amendment for entry in the above-identified application.

In the Claims:

Please amend the claims as follows:

1. (amended) A method for calculating an orthogonal discrete transform on the basis of the DIT method in prescribed intermediate steps,

wherein

a) the data are read from a memory organized on a page-for-page basis,

b) the intermediate step prescribed by the transform is carried out,

c) the resulting data are stored in a buffer memory, and

d) the resulting data are written page-for-page from the buffer memory to the memory organized on a page-for-page basis.

2. (amended) A method for calculating an orthogonal discrete transform on the basis of the DIF method in prescribed intermediate steps,

wherein

a) the data are read from a memory organized on a page-for-page basis,

b) the data are stored in a buffer memory,

c) the intermediate step prescribed by the transform is carried out, and

d) the resulting data are written page-for-page from the buffer memory to the memory organized on a page-for-page basis.

3. (amended) A method for calculating an orthogonal discrete transform on the basis of the DIF method in prescribed intermediate steps,

wherein

the data are read from two memories organized on a page-for-page basis, such that the reading is organized on a page-for-page basis, the intermediate step prescribed by the transform is carried out, and

the resulting data are again written page-for-page to the two memories organized on a page-for-page basis.

4. (amended) The method as claimed in claim 1, wherein the discrete orthogonal transform is formed by an FFT, IFFT, DCT or IDCT.

7. (amended) An apparatus for carrying out the method as claimed in claim 1 wherein

the apparatus has a memory organized on a page-for-page basis, a processor and a directly organized memory which is arranged downstream of the processor.

8. (amended) An apparatus for carrying out the method as claimed in claim 1 wherein

the apparatus has a memory organized on a page-for-page basis, a processor and a directly organized memory which is arranged upstream of the processor.

9. (amended) The apparatus as claimed in claim 7, wherein the page-oriented memory is a large memory in relation to the directly organized buffer memory.

10. (amended) The apparatus as claimed in claim 9, wherein a fast memory is used for the buffer memory.

11. (amended) The apparatus as claimed in claim 7, wherein the page-oriented memory is a dram and buffer memory is an SRAM.

12. (amended) The apparatus as claimed in claim 7, wherein the page-oriented memory has a size of 8 K addresses and the buffer memory has a size of 32 - 64 addresses.

13. (amended) An apparatus for carrying out the method as claimed in claim 3 wherein

the apparatus has two memories organized on a page-for-page basis and a processor.

14. (amended) The apparatus as claimed in claim 13, wherein the page-oriented memories are of the same size.

15. (amended) The apparatus as claim in claim 14, wherein the page-oriented memory has a size of 4 K addresses.

16. (amended) The apparatus as claimed in claim 7, wherein the processor provides a Butterfly.

IN THE SPECIFICATION:

Please add the attached Abstract to the specification.

Respectfully submitted,

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Dated: July 18, 2001

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (amended) A method for calculating an orthogonal discrete transform on the basis of the DIT method in prescribed intermediate steps,

wherein

a) the data are read from a memory [(1)] organized on a page-for-page basis,

b) the intermediate step prescribed by the transform is carried out,

c) the resulting data are stored in a buffer memory [(5)], and

d) the resulting data are written page-for-page from the buffer memory [(5)] to the memory [(1)] organized on a page-for-page basis.

2.(amended) A method for calculating an orthogonal discrete transform on the basis of the DIF method in prescribed intermediate steps,

wherein

a) the data are read from a memory [(1)] organized on a page-for-page basis,

b) the data are stored in a buffer memory [(5)],

c) the intermediate step prescribed by the transform is carried out, and

d) the resulting data are written page-for-page from the buffer memory [(5)] to the memory [(1)] organized on a page-for-page basis.

3.(amended) A method for calculating an orthogonal discrete transform on the basis of the DIF method in prescribed intermediate steps,

wherein

the data are read from two memories [(3, 4)] organized on a page-for-page basis, such that the reading is organized on a page-for-page basis, the intermediate step prescribed by the transform is carried out, and

the resulting data are again written page-for-page to the two memories [(3, 4)] organized on a page-for-page basis.

4.(amended) The method as claimed in [one of claims 1 to 3] <u>claim 1</u>, wherein the discrete orthogonal transform is formed by an FFT, IFFT, DCT or IDCT.

7.(amended) An apparatus for carrying out the method as claimed in [one of claims 1, 4, 6] <u>claim 1</u>

wherein

the apparatus has a memory [(1)] organized on a page-for-page basis, a processor [(2)] and a directly organized memory [(5)] which is arranged downstream of the processor.

8.(amended) An apparatus for carrying out the method as claimed in [one of claims 1, 4, 6] <u>claim 1</u>

wherein

the apparatus has a memory [(1)] organized on a page-for-page basis, a processor [(2)] and a directly organized memory [(5)] which is arranged upstream of the processor.

9. (amended) The apparatus as claimed in [one of claims 7 or 8] claim 7, wherein the page-oriented memory [(1)] is a large memory in relation to the directly organized buffer memory [(5)].

10.(amended) The apparatus as claimed in claim 9, wherein a fast memory is used for the buffer memory [(5)].

11.(amended) The apparatus as claimed in [one of claims 7-10] claim 7, wherein the page-oriented memory [(1)] is a dram and buffer memory [(5)] is an SRAM.

12.(amended) The apparatus as claimed in [one of claims 7-11] claim 7, wherein the page-oriented memory [(1)] has a size of 8 K addresses and the buffer memory [(5)] has a size of 32 - 64 addresses.

13.(amended) An apparatus for carrying out the method as claimed in [one of claims 3, 4-6] claim 3

wherein

the apparatus has two memories [(3, 4)] organized on a page-for-page basis and a processor [(2)].

14.(amended) The apparatus as claimed in claim 13, wherein the page-oriented memories [(3, 4)] are of the same size.

15.(amended) The apparatus as claim in claim 14, wherein the page-oriented memory [(3, 4)] has a size of 4 K addresses.

16.(amended) The apparatus as claimed in [one of claims 7-15] claim 7, wherein the processor [(2)] provides a Butterfly.

Description

Method and apparatus for calculating a discrete orthogonal transform such as FFT or IFFT

The invention relates to a method and a circuit for calculating the fast Fourier transform and also the inverse transform thereof, called FFT and IFFT below, or transforms of similar structure, i.e. discrete orthogonal transforms.

The FFT and IFFT are extremely important transforms in communications technology because, by way of example, they transform the description of a factual basis in the time domain into a factual basis in the frequency domain, and vice-versa.

In digital signal processing, an 'N point' discrete Fourier transform, called DFT below, is frequently calculated which is defined as follows:

$$X(k) = \sum_{n=0}^{N-1} x(n)\ W^{nk} \qquad k = 0, 1, \ldots, N-1$$

where $W = e^{(-j)2\pi/N}$

The complexity of calculating the DFT is proportional to $O(N^2)$. By using the FFT, it is possible to reduce the complexity of the calculation to $O(N\log(N))$. This is done by hierarchical splitting of the calculation into transforms having shorter successions.

To calculate the FFT, there are two basic algorithms. One is called "Decimation in Frequency" (DIF) and the other is called "Decimation in Time" (DIT). The text below deals with the DIT algorithm by way of example.

To calculate the FFT, the "in-place" variant is preferably used in which calculated intermediate results of the Butterfly calculation are written to the same memory, from where they are in turn read and put to further use, as shown in figure 1. This provides for particularly economical use of the memory.

Figure 2 shows the calculation operation of the "in-place" variant for N = 8 in the form of a signal flowchart. As can be seen from figure 2, at the start of the calculation, the memory needs to contain the data in a particular arrangement, usually referred to as "bit-reversed". At the end of calculation, the result can be read linearly. The calculation itself is performed in a plurality of stages, as shown in the signal flowchart in figure 2. In the cited example, three stages are necessary. In each case, two data items are read from the memory, the Butterfly is then calculated, and the two results are written back again to the same locations in the memory. In this context, the data items are not necessarily situated in adjacent memory locations, however. In addition, the calculation differs from one stage to the next.

If the FFT is implemented in integrated circuits, the complexity is primarily determined by the memory used. In this context, large memories are usually of page-for-page design, which means that access to a memory cell within such a page is very fast; by way of example, such a memory access operation can be carried out within one clock cycle. Changing from one page to another takes significantly longer, however, i.e. a plurality of clock cycles. It is possible to increase the throughput in page-oriented memories by processing a page of a memory as completely as possible and only then changing the page again, because addresses of the other page are required. In the case of the aforementioned "in-place" FFT, however, the data are,

in principle, required in very unorganized form. Small memories do not have this drawback, since access to the individual cells is possible without restriction in this case.

The speed of the FFT is therefore primarily limited by the interface to the memory.

The invention is therefore based on the object of providing a method and an apparatus for calculating discrete orthogonal transforms, in particular the FFT and IFFT, which permit faster calculation.

The object is achieved by the features of the independent claims. Preferred refinements of the invention are the subject matter of the subclaims.

The first inventive method for calculating an orthogonal discrete transform on the basis of the DIT method in prescribed intermediate steps, where an intermediate step is to be understood as meaning the addition and multiplication of a processing stage, comprises the following steps:

a) the data are read from a memory organized on a page-for-page basis,
b) the intermediate step prescribed by the transform is carried out,
c) the resulting data are stored in a buffer memory, and
d) the resulting data are written page-for-page from the buffer memory to the memory organized on a page-for-page basis.

The inventive method for calculating an orthogonal discrete transform on the basis of the DIF method in prescribed intermediate steps has the following steps:

a) the data are read from a memory organized on a page-for-page basis,

b) the data are stored in a buffer memory,

c) the intermediate step prescribed by the transform is carried out, and

d) the resulting data are written page-for-page from the buffer memory to the memory organized on a page-for-page basis.

A third inventive method for calculating an orthogonal discrete transform in prescribed intermediate steps has the following steps:

a) the data are read from two memories organized on a page-for-page basis, so that the reading is organized on a page-for-page basis,

b) the intermediate step prescribed by the transform is carried out, and

c) the resulting data are written page-for-page to the two memories organized on a page-for-page basis.

Examples of a suitable discrete orthogonal transform are an FFT, an IFFT, a DCT or an IDCT and also transforms organized on a schematically similar basis.

Preferably, the transform has an identical geometry for each stage, which facilitates the addressing of the results. By way of example, this condition is satisfied for an FFT or an IFFT based on Singleton.

In accordance with the above methods, the inventive apparatuses have

a memory organized on a page-for-page basis, a processor and a directly organized memory which is arranged downstream of the processor, or

a memory organized on a page-for-page basis, a processor and a directly organized buffer memory which is arranged upstream of the processor, or

two memories organized on a page-for-page basis and a processor.

In this context, the processor provides a "Butterfly".

Preferred embodiments of the invention are explained below with reference to the drawings.

Figure 1 shows the diagram for calculation of an "in place" FFT,

Figure 2 shows the signal flowchart for an "in place" FFT for N = 8,

Figure 3 shows the signal flowchart for a "Singleton" FFT for N = 8,

Figure 4 shows a first embodiment for calculating an FFT, and

Figure 5 shows a second embodiment for calculating an FFT on the basis of the DIT method.

Figure 1 shows the aforementioned usual "in-place" calculation of an FFT, where a data pair is read from a memory 1, normally a DRAM, is logically combined in a Butterfly unit 2 and is written to the memory 1 again.

Figure 2 shows the basic DIT algorithm for an FFT calculation for N = 8. For calculation, the data items x(0) to x(7) need to be present in the memory in "bit-reversed" fashion at the start. The figure shows the signal flowchart for calculating the Fourier components X(0) - X(7). The algorithm and the signal flowchart are described in A.V. Oppenheim, R.W. Schafer: "Digital Signal Processing", Prentice-Hall Inc., Englewood Cliffs, New Jersey, USA, 1975, pp. 285 ff., so that there is no need for this to be explained in more detail here. With regard to the nomenclature, the factors W^0, W^1 and W^2 are also called twiddle factors.

Figure 3 shows an FFT algorithm with an altered sequence of computation operations, the "Singleton algorithm", which is described on page 301 of the aforementioned literature reference Oppenheim-Schafer and is used in the method according to the invention. It is clear to see that the data are processed in very regular fashion, but no "in place" processing is carried out. Twice the memory space as compared with the "in place" calculation is therefore required.

Advantageously, the calculation has entirely the same structure in each stage, with the exception of the twiddle factors. This means that the stages of the illustrative algorithm for an FFT for N = 8 have an identical geometry. When a stage has been processed, the last memory written to is read and another memory is written to.

The memory can be read linearly. Linear writing is not yet possible in the algorithm, however, since it is always necessary to store one result in the top half (solid line) and one result in the bottom half (dashed line). However, linear writing is possible in the top and bottom halves.

Figure 4 shows a schematic illustration of a first inventive embodiment for rapidly calculating an algorithm which has a similar or the same design as the Singleton algorithm shown in figure 3. [lacuna] Such an apparatus, which is suitable both for DIF and DIT calculation, the memory required for the calculation is subdivided into two page-oriented memories 3, 4 which are of the same size and are in the form of DRAMs (DRAM = Dynamic RAM). The use of two page-oriented memories 1 and 2 means that each memory can inherently be written to in linear fashion, i.e. a respective memory is used for the top and bottom halves of the algorithm shown in figure 3, so that the number of slow page changes is

small. The number of memories and the number of interfaces are doubled, however.

A second embodiment, shown in figure 5, for rapidly calculating a DIT transform like that in figure 3 is the use of a small fast memory 5 arranged downstream of the Butterfly 2. This memory buffer-stores a few intermediate results of the calculation so that it can then write them to the page-oriented memory 1 without constantly changing page. The course of the calculation is now that two data items are read from the memory 1, are supplied to the Butterfly, and the intermediate results are stored in the fast SRAM memory 5 (SRAM = Static RAM). The intermediate results are then written page-for-page to the page-oriented memory 1.

In the case of calculation on the basis of the DIF method, the static fast memory 5 is situated at the input of the Butterfly 2 (not shown). In other respects, the manner of operation is similar to that of the DIT variant explained.

The table 1 below illustrates the addressing scheme for calculation using buffer-storage:

Table 1

DRAM (RD)	Butterfly	SRAM (WR)	SRAM (RD)	DRAM (WR)
0	0	0		
1	16	8		
2	1	1		
3	17	9		
4	2	2	0	0
5	18	10	1	1
6	3	3	2	2
7	19	11	3	3
8	4	4	8	16

9	20	12	9	17
10	5	5	10	18
11	21	13	11	19
12	6	6	4	4
13	22	14	5	5
14	7	7	6	6
15	23	15	7	7
16	8	0	12	20
17	24	8	13	21
18	9	1	14	22
19	25	9	15	23
20	10	2	0	8
21	26	10	1	9
22	11	3	2	10
23	27	11	3	11
24	12	4	8	24
25	28	12	9	25
26	13	5	10	26
27	29	13	11	27
28	14	6	4	12
29	30	14	5	13
30	15	7	6	14
31	31	15	7	15
			12	28
			13	29
			14	30
			15	31

In the example, the page-oriented memory has a depth of N = 32, which means that an FFT having 32 points can be calculated. A page of the slow page-oriented memory may have P = 4 addresses, for example, and the fast memory used may have a size of $S = 4 \cdot P = 16$ addresses. The data can be read linearly in the order 0, 1, 2, ... By way of example, for the purposes of processing, the Butterfly reads (RD) the data for the DRAM addresses 0 and 1. The intermediate results of the Butterfly

produce addresses 0 and 16. These are written (WR) to the addresses 0 and 8 of the fast buffer memory SRAM. With a delay which is required for partly filling the memory, the data are read page-for-page in linear fashion, that is to say, in table 1, under SRAM (RD) the addresses 0-3, then 8-11 etc. The content of these SRAM addresses is written page-for-page in linear fashion to the appropriate addresses, which are conditional on the transform, of the slow page-oriented memory (column DRAM (WR)), that is to say on the basis of 0-3, 16-19, 4-7 etc., in the example. The use of the small fast memory therefore optimizes access to the page-oriented memory DRAM such that the slow page changes required are as few as possible.

The transforms and memory sizes mentioned above and explained serve only as an illustration. In practice, the slow memory is much larger than the fast memory. By way of example, the slow memory is normally designed for N = 8192, with the slow memory having a page size of P = 16. The small memory therefore has a size of 64 addresses. In an integrated implementation, the fast small memory is therefore of barely any consequence in terms of surface area, but calculation of the FFT or IFFT or of similar discrete orthogonal transforms is significantly speeded up on account of the minimization of the page changes in the slow memory.

List of reference numerals

1 Page-oriented memory
2 Butterfly
3 Page-oriented memory
4 Page-oriented memory
5 Fast memory

Patent claims

1. A method for calculating an orthogonal discrete transform on the basis of the DIT method in prescribed intermediate steps,
wherein
   a) the data are read from a memory (1) organized on a page-for-page basis,
   b) the intermediate step prescribed by the transform is carried out,
   c) the resulting data are stored in a buffer memory (5), and
   d) the resulting data are written page-for-page from the buffer memory (5) to the memory (1) organized on a page-for-page basis.

2. A method for calculating an orthogonal discrete transform on the basis of the DIF method in prescribed intermediate steps,
wherein
   a) the data are read from a memory (1) organized on a page-for-page basis,
   b) the data are stored in a buffer memory (5),
   c) the intermediate step prescribed by the transform is carried out, and
   d) the resulting data are written page-for-page to the memory (1) organized on a page-for-page basis.

3. A method for calculating an orthogonal discrete transform in prescribed intermediate steps,
wherein
the data are read from two memories (3, 4) organized on a page-for-page basis such that the reading is organized on a page-for-page basis,
the intermediate step prescribed by the transform is carried out, and

the resulting data are again written page-for-page to the two memories (3, 4) organized on a page-for-page basis.

4. The method as claimed in one of claims 1 to 3, wherein the discrete orthogonal transform is formed by an FFT, IFFT, DCT or IDCT.

5. The method as claimed in claim 4, wherein the transform has an identical geometry for each stage.

6. The method as claimed in claim 5, wherein an FFT or IFFT based on Singleton is used.

7. An apparatus for carrying out the method as claimed in one of claims 1, 4-6,
wherein
the apparatus has a memory (1) organized on a page-for-page basis, a processor (2) and a directly organized memory (5) which is arranged downstream of the processor.

8. An apparatus for carrying out the method as claimed in one of claims 2, 4-6,
wherein
the apparatus has a memory (1) organized on a page-for-page basis, a processor (2) and a directly organized buffer memory (5) which is arranged upstream of the processor.

9. The apparatus as claimed in one of claims 7 or 8, wherein the page-oriented memory (1) is a large memory in relation to the directly organized buffer memory (5).

10. The apparatus as claimed in claim 9, wherein a fast memory is used for the buffer memory (5).

11. The apparatus as claimed in one of claims 7-10, wherein the page-oriented memory (1) is a DRAM and the buffer memory (5) is an SRAM.

12. The apparatus as claimed in one of claims 7 - 11, wherein the page-oriented memory (1) has a size of 8 K addresses and the buffer memory (5) has a size of 32 - 64 addresses.

13. An apparatus for carrying out the method as claimed in one of claims 3, 4-6, wherein the apparatus has two memories (3, 4) organized on a page-for-page basis and a processor (2).

14. The apparatus as claimed in claim 13, wherein the page-oriented memories (3, 4) are of the same size.

15. The apparatus as claimed in claim 14, wherein the page-oriented memory (3, 4) has a size of 4 K addresses.

16. The apparatus as claimed in one of claims 7 - 15, wherein the processor (2) provides a Butterfly.

Fig. 1

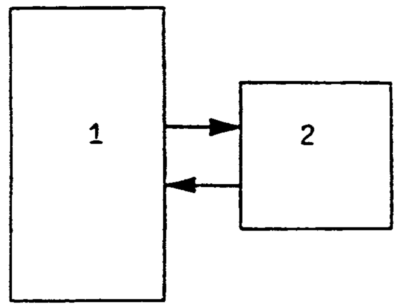


Fig. 2

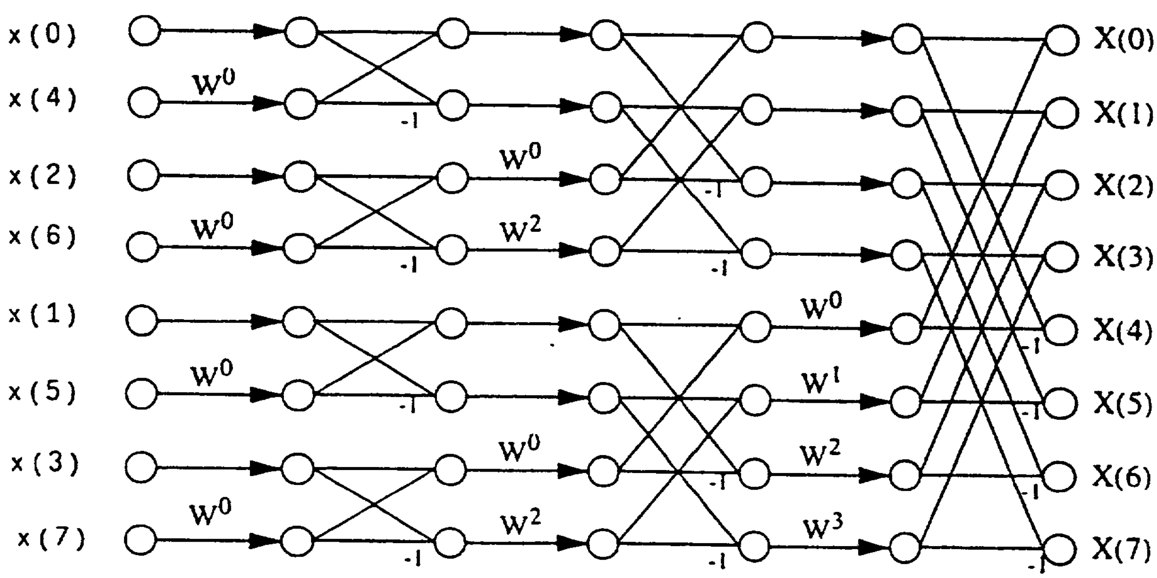


Fig. 3

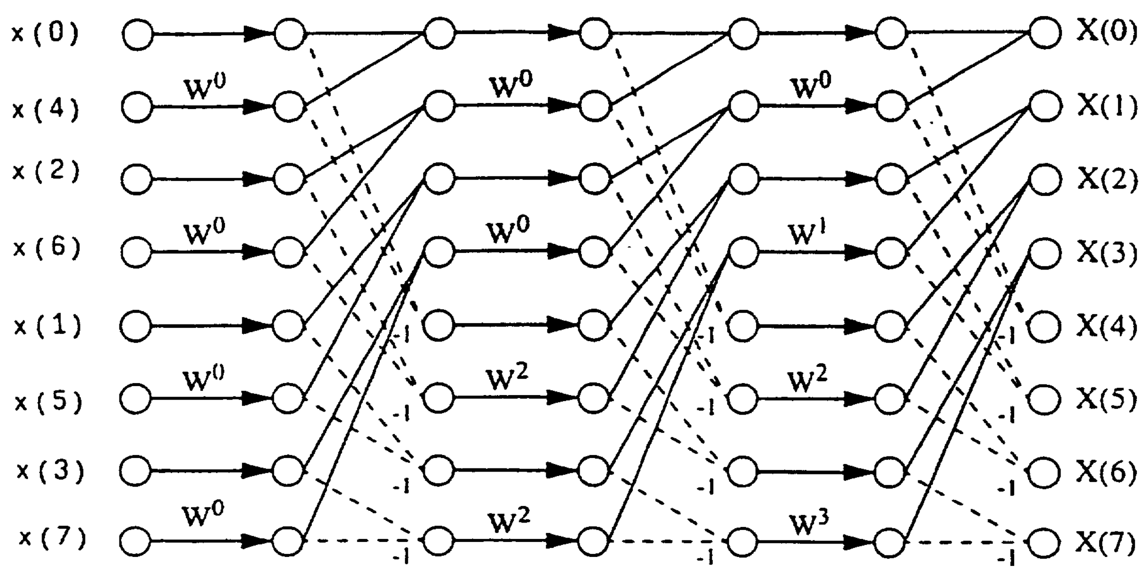


Fig. 4

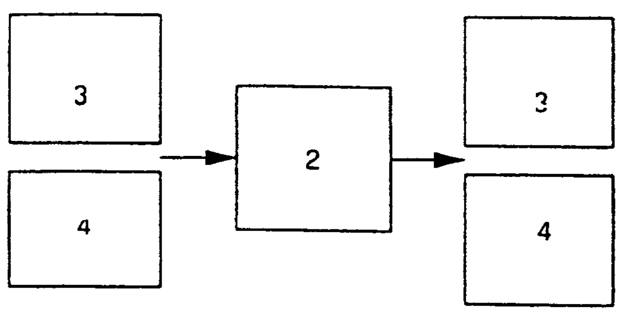
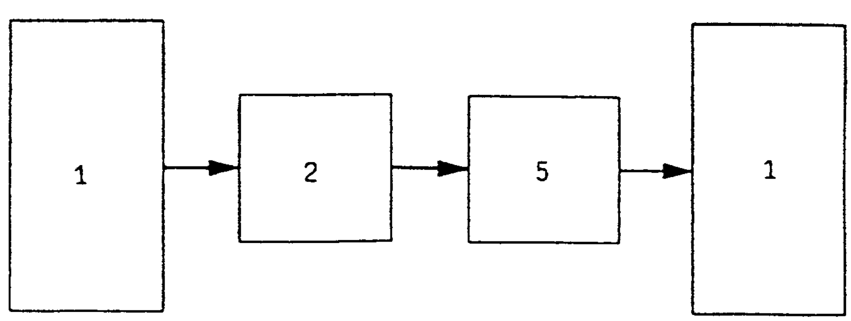


Fig. 5



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DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare:

That my residence, post office address and citizenship are as stated below next to my name.

That I verily believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: **METHOD AND DEVICE FOR CALCULATING A DISCRETE ORTHOGONAL TRANSFORMATION SUCH AS FFT OR IFFT** the specification of which (check one)

☒ is attached hereto.

☐ was filed on as Application, Serial No. and was amended on ______________ (if applicable).

That I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

That I acknowledge the duty to disclose information known to be material to patentability of this application in accordance with Title 37, Code of Federal Regulations §1.56(a).

That I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate on this invention having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)

(Number)	(Country)	(Day/Month/Year Filed)	Priority Claimed
199 06 868.2	Germany	18/02/1999	☒ Yes ☐ No
WO 00/49518	PCT	24/08/2000	☒ Yes ☐ No

That I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

United States Application(s)

(Application Serial No.)	(Filing Date)	(Status)-(Patented, pending, abandoned)

That all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

I hereby appoint the following attorneys, with full power of substitution and revocation, to prosecute this application and to transact all business in the United States Patent and Trademark Office connected therewith and request that all correspondence and telephone calls in respect to this application be directed to: WELSH & KATZ, LTD., 120 South Riverside Plaza, 22nd Floor, Chicago, Illinois 60606-3913, Telephone No.: (312) 655-1500:

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I hereby authorize the U.S. attorney or agent named herein to accept and follow instructions from Reinhard, Skuhra, Weise & Partner GbR as to any action to be taken in the Patent and Trademark Office regarding this application without direct communication between the U.S. attorney or agent and the undersigned. In the event of a change in the persons from whom instructions may be taken, I will so notify the U.S. attorney or agent named herein.

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